CHIPS NAPMP: Overview and Next Steps

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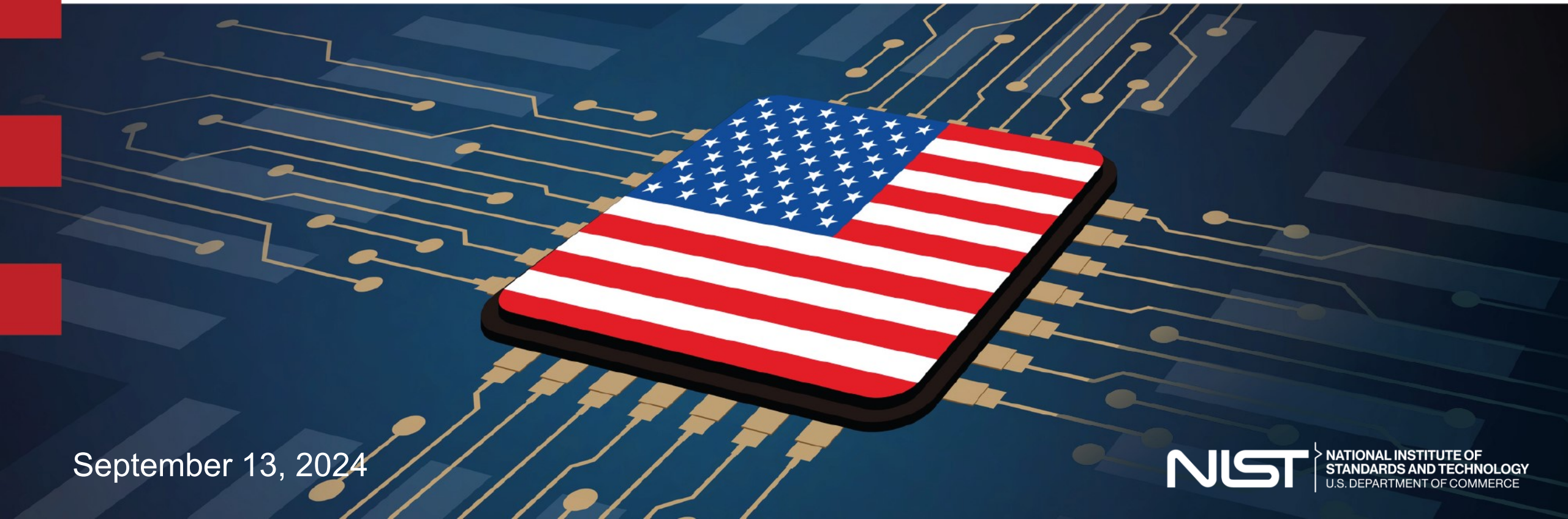
IEEE ESTC Conference



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NIST NATIONAL INSTITUTE OF STANDARDS AND TECHNOLOGY
U.S. DEPARTMENT OF COMMERCE

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  - Do not constitute a commitment and are not binding on NIST or the Department of Commerce.
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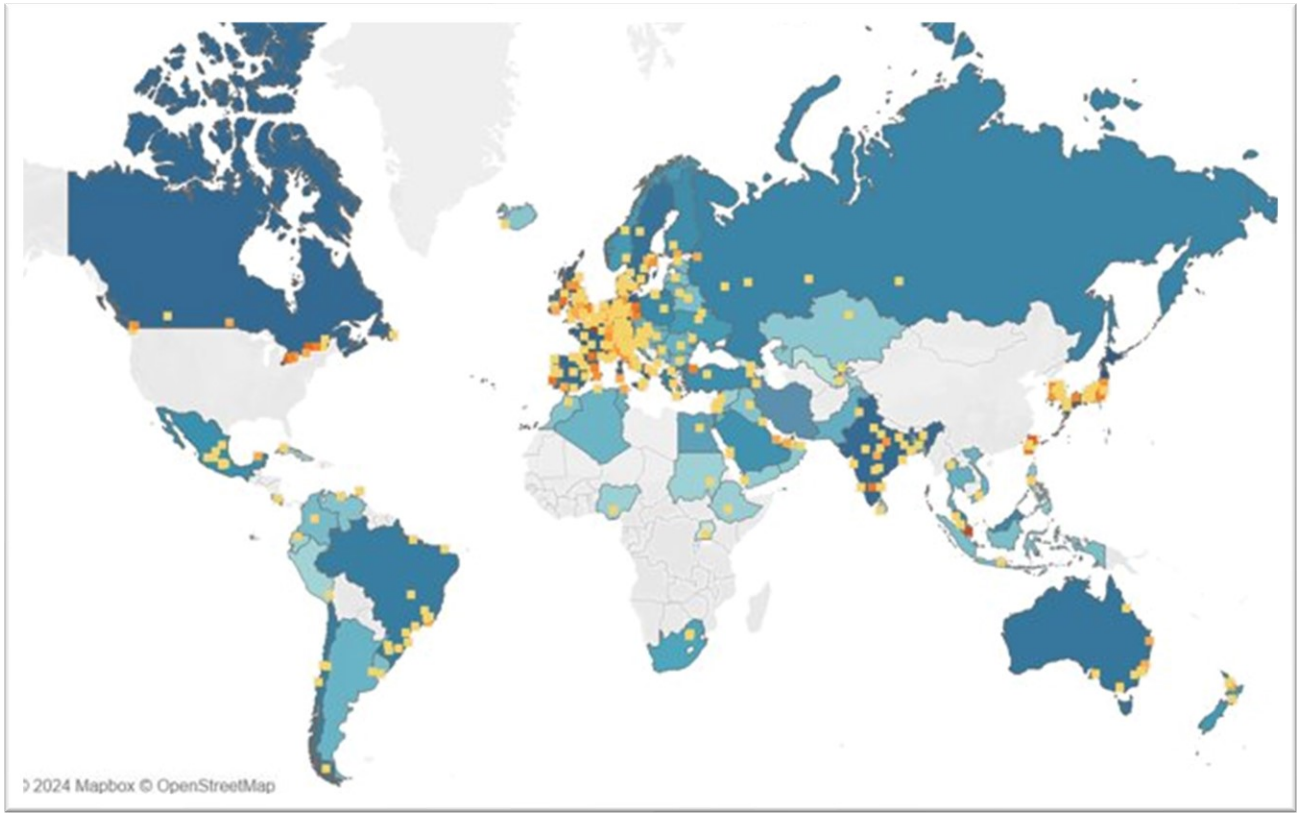
- Nothing in this presentation is intended to contradict or supersede the requirements published in any future policy documents or funding opportunities.

R&D International Landscape

- Semiconductor R&D ecosystem and supporting supply chains span the globe
- International cooperation on common challenges can advance specific goals, expand infrastructure access, and enable new solutions
- Expanding and emerging innovation clusters leading the world (Hsinchu, Paris, Seoul, Singapore, Tokyo, others)



*Global semiconductor R&D map drawn from R&D patent filings and published research from 2000-2024 outside U.S. and China

CHIPS for America

$39 billion for incentives

Two component programs to:

1. Attract large-scale investments in advanced technologies such as leading-edge logic and memory, and advanced packaging
2. Incentivize expansion of manufacturing capacity for mature and other types of semiconductors

$11 billion for R&D

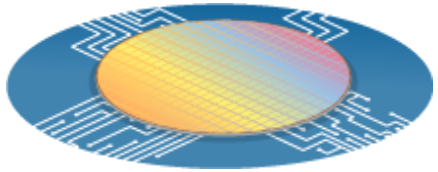
Four integrated programs to:

1. Conduct research and prototyping of advanced semiconductor technology
2. Strengthen semiconductor advanced packaging, assembly, and test
3. Enable advances in measurement science, standards, material characterization, instrumentation, testing, and manufacturing

$2 billion for DoD Microelectronics Commons

A national network that will create direct pathways to commercialization for US microelectronics researchers and designers from “lab to fab.”

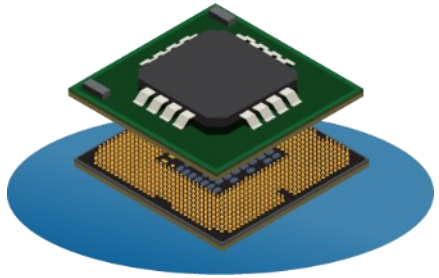
CHIPS R&D Programs



CHIPS National Advanced Packaging Manufacturing Program (NAPMP)

Manufacturing USA

CHIPS Manufacturing USA Program



CHIPS National Semiconductor Technology Center (NSTC) Program

Natcast

Natcast is a purpose-built, nonprofit organization and operator of the NSTC consortium

CHIPS Metrology Program

Workforce Initiatives

U.S. Engagement with International Partners

U.S.-led International Dialogues on Semiconductors

Americas

- Canada
- Costa Rica
- Mexico
- Uruguay

East Asia

- Japan
- Korea
- Malaysia
- Singapore
- Taiwan

Europe

- Netherlands
- United Kingdom

Multilateral

- G7
- EU

South Asia

- India

Supporting U.S. Initiatives

CHIPS for America

- R&D Office and Program Office staff leading international engagement in support of $50 billion in U.S. programs

International Technology and Security Innovation (ITSI) Fund

- $500 million over five years under U.S. Department of State for international engagement

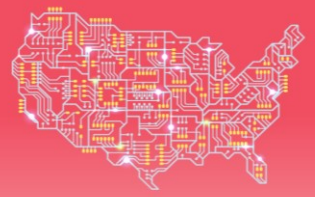
2-Year Progress Report

Total committed by the Biden-Harris Administration: $30+ billion in proposed incentives funding

PROPOSED
$30+ billion
IN INCENTIVES FUNDING

UNLEASHED
$300+ billion
IN PRIVATE INVESTMENTS

All five major leading-edge logic and DRAM companies will produce chips in the U.S.

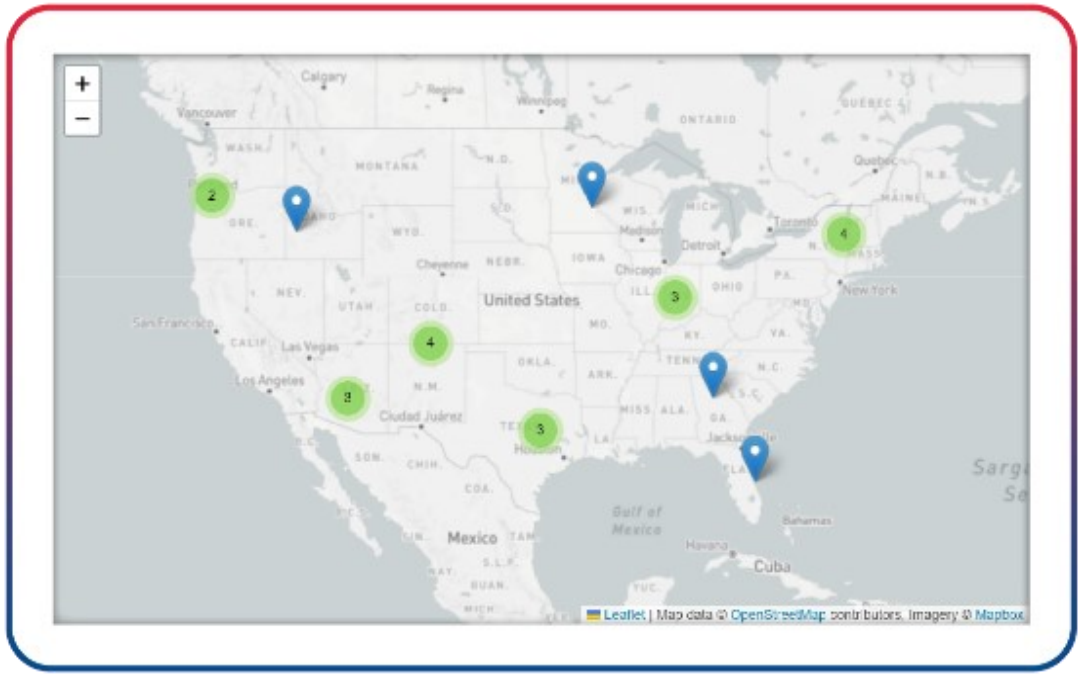


No other economy in the world has more than two

115,000+ jobs

35,000+ manufacturing jobs

78,000+ construction jobs



https://www.nist.gov/chips/funding-updates

NAPMP Vision, Mission, and Outcomes

Vision

The National Advanced Packaging Manufacturing Program will drive **U.S. leadership** in advanced packaging and provide the technology needed for packaging manufacturing in the United States.

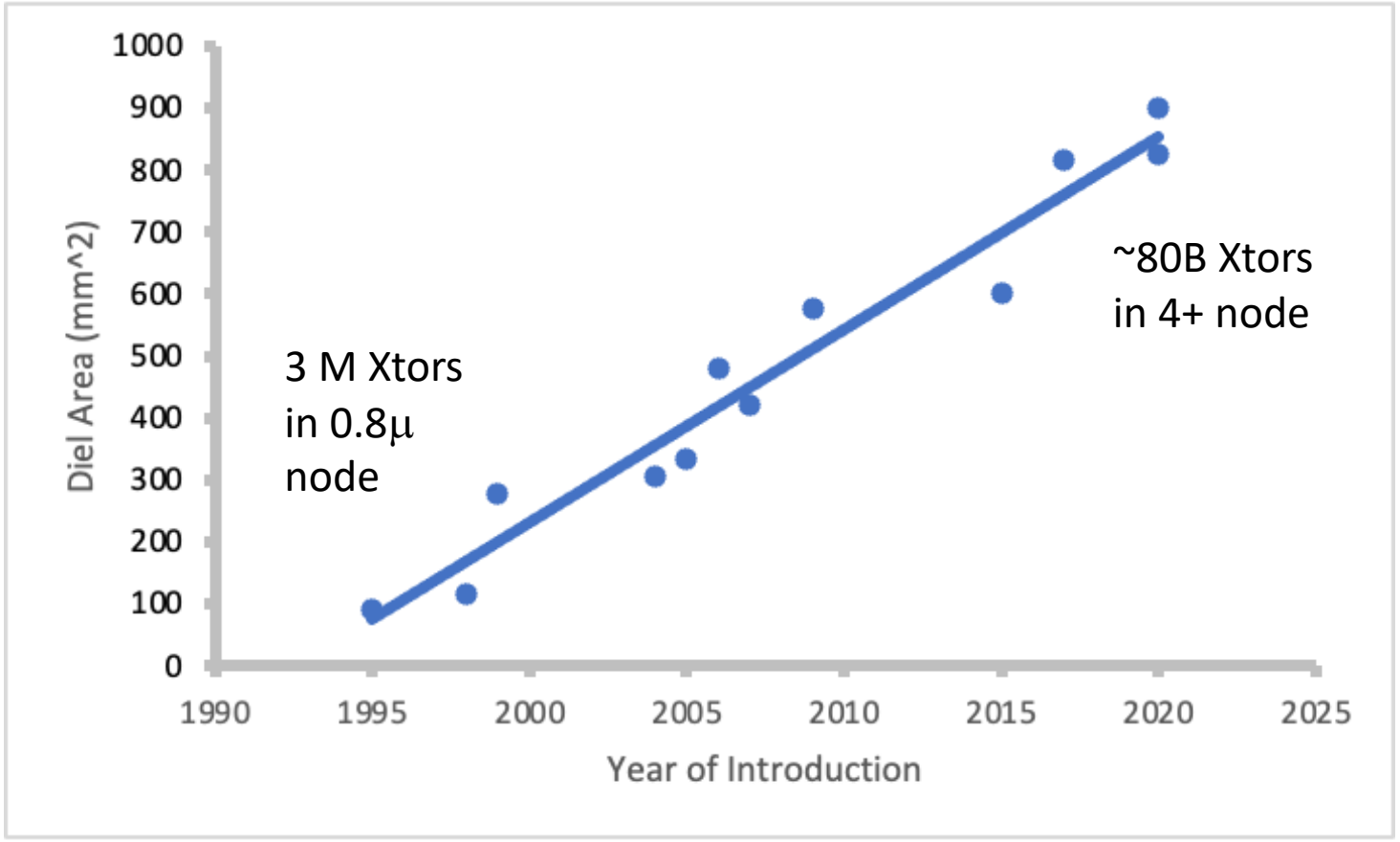
Mission

The NAPMP will develop **critical and relevant innovations** for advanced packaging technologies and **accelerate their scaled transition** to U.S. manufacturing entities.

Outcomes

- Within a decade, NAPMP-funded activities, **coupled with CHIPS manufacturing incentives,** will establish a vibrant, self-sustaining, profitable, high-volume, domestic, advanced packaging industry where advanced-node chips manufactured in the U.S. are packaged in the U.S.
- We expect the technology developed to be leveraged in new applications and market sectors and at scale.

Even though transistors have scaled dramatically, die sizes have grown larger



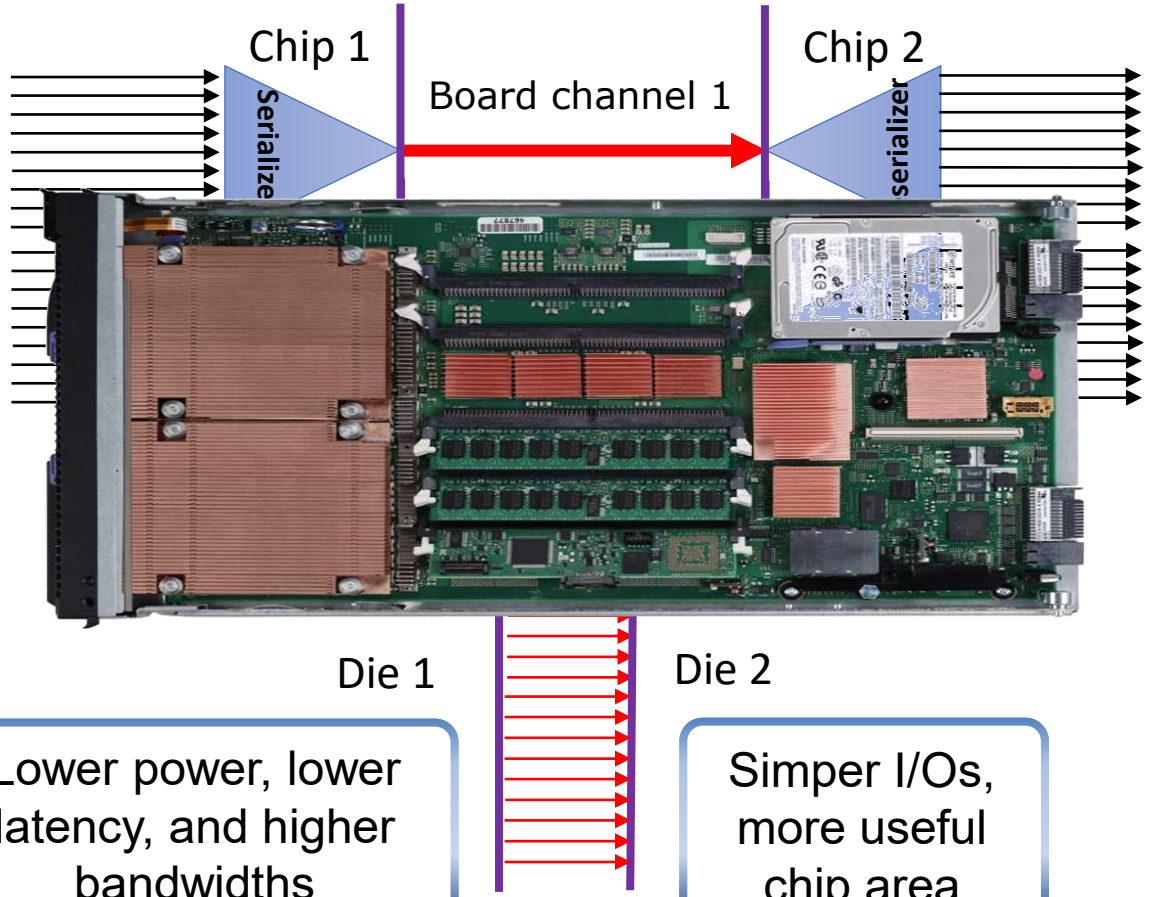
This chart shows past and current die size scaling trend

- Monolithic dies still outperform multi-chip packaged assemblies
  - Because packaging scaling has not kept up with silicon scaling (~10X Vs 10^6 X)
  - But high-performance dies have reached reticle limits
- Packaging is evolving to emphasize system integration rather than single chip packaging with the increasing adoption of silicon processing techniques

**Die size data from commercial product spec sheets*

Heterogeneous integration is not new

The difference now is scale:



Lower power, lower latency, and higher bandwidths

Simper I/Os, more useful chip area

- More channels on the package
  - Finer ”bump/pillar” pitch
  - Approach on-chip via pitches (<1 µm)
- Finer trace pitch
  - Approach on-chip wiring pitches
- Shorter inter-die distance
  - ~ µm

Scale Down

- Significantly more intimately connected silicon

Scale Out

Advanced packaging blurs the line between a monolithic chip and a packaged assembly of heterogeneous chips

Scaling down features on the package:

- Making the features on the package approach those at the top level on a monolithic CMOS chip
- Connecting the dies to the package at pitches approaching the final via pitches on a chip
- Reducing the distance between dies that are assembled on a multi-chip package to approach the distance between IP blocks on a monolithic chip

Scaling out the package

- Accommodate a larger number of closely packed heterogeneous dies
- Address the power delivery, thermal dissipation, and external connection challenges
- Develop standards and protocols to accommodate this large and diverse set of chips (chiplets)

Establishing Advanced Packaging in the U.S.

Packaging Roadmaps

- NIST sponsored roadmaps: MRHIEP, MAESTRO and MAPT
- Other roadmaps: HIR and IRDS

Technology R&D Areas

- All aspects of technologies required to develop a leading-edge on-shore advanced packaging manufacturing capability

The National Advanced Packaging Piloting Facility (NAPPF)

- Validates & practices NAPMP thrusts
- Piloting and prototyping functions

The Chiplet and Design Ecosystem

- Chiplet discovery, disaggregation and reaggregation methodologies, protocols, standards, fabrication and warehousing design for test, repair and reliability and holistic design tools and methodologies

Design in the U.S., build in the U.S., and Sell Worldwide

- Prototyping packaging flows to be implemented in the NAPPF

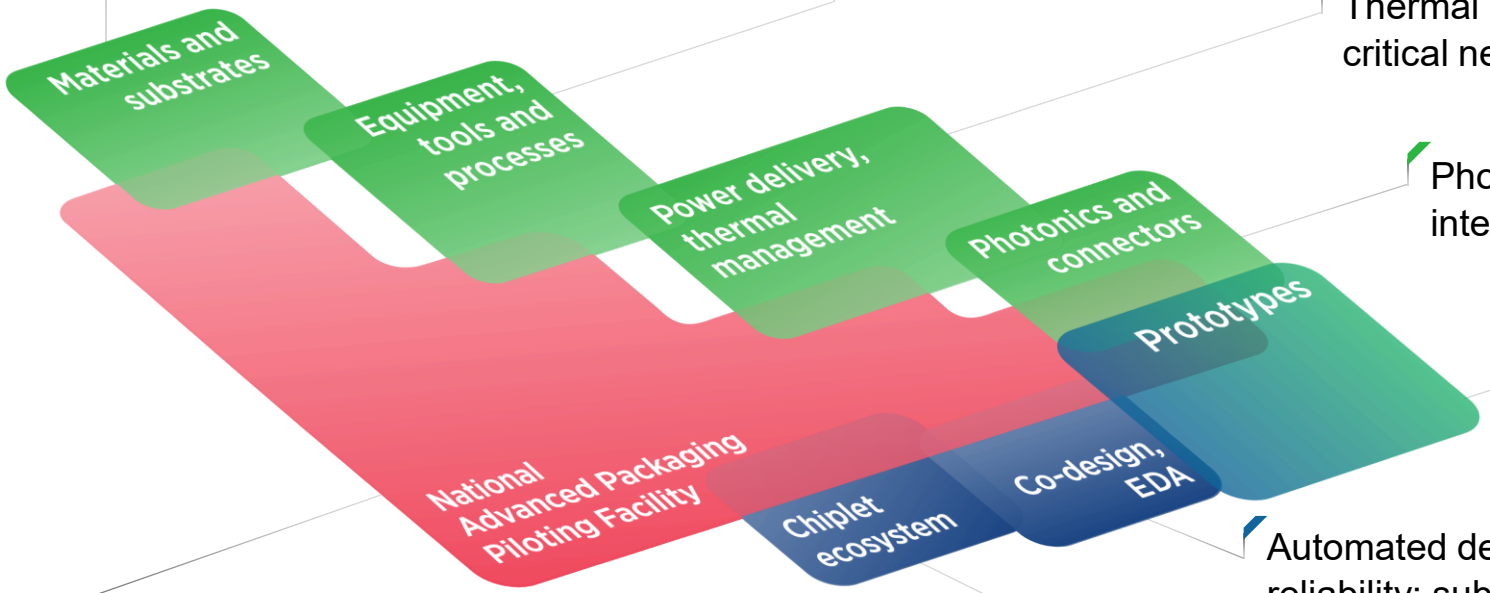
NAPMP Structure: six hardware and eco-system thrusts + piloting facility + prototyping challenges

Substrates & materials are the platform for heterogeneous integration of dielets

Equipment, tools & processes are needed to pattern substrates and assemble dielets and passivate assemblies

Thermal management and efficient power delivery are critical needs

Photonics and connectors allow the assembly to interact with the outside world



Functional prototypes that leverage advanced packing process flows in the areas of high performance and low power and that validate the processes installed in the NAPMP Piloting Facility

Automated design for test, repair, security, and reliability; substrate and process dependent

The chiplet eco system is crucial for any implementation of advanced packaging

The NAPMP Piloting Facility provides a test bed for integration of the different investment areas and also functions as a piloting and prototyping facility

NOFO 1: Materials and Substrates

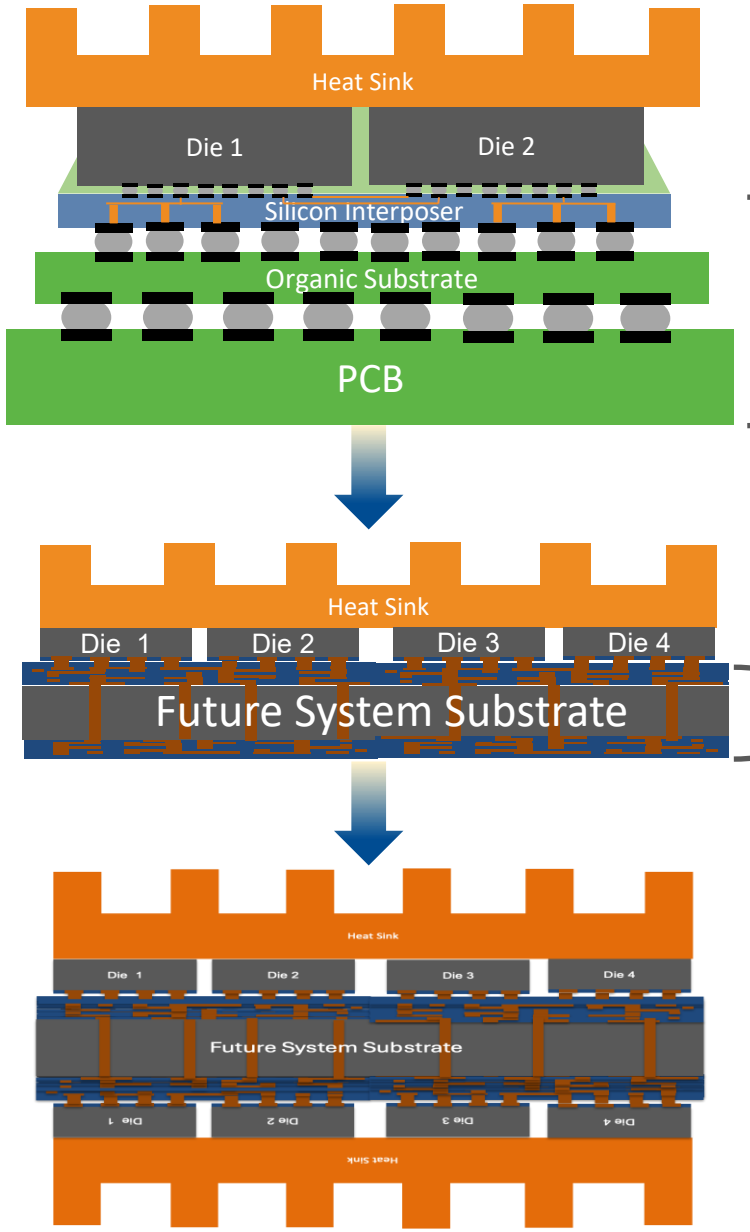
"The key requirements of new substrates include multiple levels of fine wiring and via pitches, low warpage, large area, and the ability to integrate active and passive components."

- Materials and substrates are the platform on which advanced packaging is built.
- These substrates or interconnect fabrics (IF) may be based on silicon, glass, or organic materials and can include fan-out wafer-level processes.
- The IF needs to be
  - compatible with advanced and legacy nodes and different semiconductor material systems
  - have integrable active and passive components
  - compatible with either mass reflow, thermal compression bonding or hybrid bonding
- Meet environmental and sustainability goals

From 11/27 Webinar

In NOFO1 Materials and Substrates

- We addressed Substrates
- We solicited proposals in three broad areas:
  - Organic based substrates
  - Glass based substrates
  - Semiconductor based substrates
- We had very aggressive targets on substrate wiring pitch and the pitch at which we expected dielets to be attached to these substrates
- The goal was to as far as possible use these substrates to build a flat hierarchy without interposers
- And integrate thermal dissipation or even two-sided assembly



From Proposers Day

R&D Areas

Equipment, tools, processes and process integration

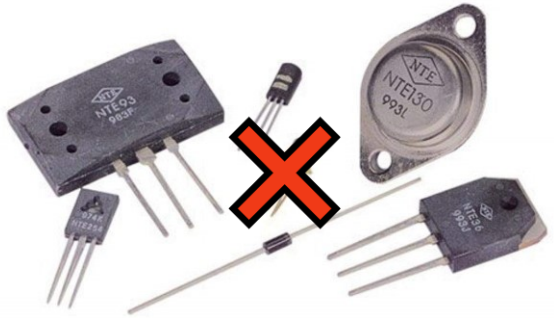
- **Focus:** Develop end-to-end packaging flows that enable a chiplet-based advanced packaging architecture suitable for commercial adoption
- Aggressive bond-pitch scaling and alternate assembly methods require innovations in process technologies and fabrication equipment to achieve high yields and cost-effective volume manufacture
- R&D to center on process clusters, defined as sequences of steps that enable a key part of the packaging flow:
  - *Chiplet singulation*: Low damage, high-precision methods to produce singulated chiplets from wafers
  - *Chiplet to substrate bonding*: Methods to attach chiplets with ultra-fine-pitch bonding pads to substrates, that enable the transition to solder-free interconnects (e.g., Cu-Cu)
  - Enhanced through-silicon via (TSV) processes
  - *3-dimensional heterogeneous integration (3DHI)*: Form heterogeneous chiplet stacks with ultra-fine bonding pad pitches, for inclusion in the packaged device
  - *Collective Chiplet Processing*: Placing arrays of singulated chiplets on a carrier, to be compatible with NAPMP-funded assembly techniques specified in the NOFO
  - *Finishing*: Incorporating advanced power delivery, passivation, thermal management, and connectors, including photonics, into the packaged device
- Comprehensive R&D approaches that encompass interactions between steps, step sequencing within each cluster, equipment factors, and manufacturability are recommended

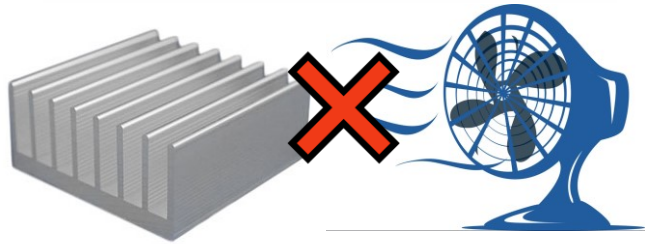
Power Delivery and Thermal Management

It is expected that proposals within this area may consider related research challenges within other R&D areas, such as Co-design/Electronic Design Automation (EDA) and the Chiplets Ecosystem.

Vertical heat extraction, local heat spreading, advanced methods for active and passive cooling of 3DHI devices to reliably operate at higher power density, wide bandgap chiplets for 3DHI, and advanced materials and architectures to achieve specific thermal and power goals such as low-resistance thermal interfaces are in scope.

Expected to be out of scope in this R&D area are discrete packaged wide bandgap devices and conventional air-cooling approaches.





https://www.amazon.com/NTE-Electronics-NTE4060B-Integrated-Oscillator/dp/B0002FREZW
https://www.vectorstock.com/royalty-free-vector/fan-vector-16718180

Power Delivery and Thermal Management

Address challenges introduced by advanced packaging in terms of power delivery, power efficiency, and thermal management.

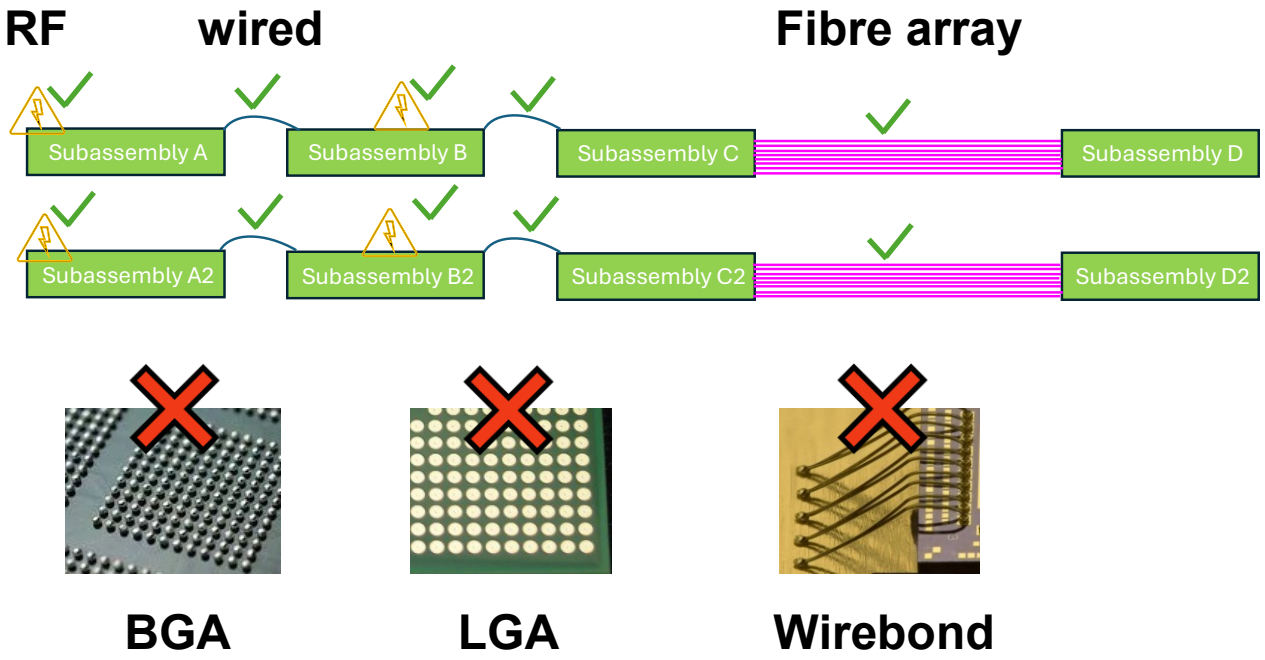
Expected Projects would address one or more of the following:

1. New thermal solutions – for implementation with advanced substrates, 3D heterogeneous integration (3DHI), and other design aspects – to reduce hotspots, maintain thermal targets, and enable reliability in multilayer stacks without constraining connectivity.
2. Innovative approaches for delivering power at high density with efficient voltage regulators and dynamic power management schemes for 3DHI devices, including modular designs and devices for use with a variety of chiplets.
3. Validated, higher fidelity models and accelerated learning using artificial intelligence and machine learning (AI/ML) to accurately predict power and thermal distributions across chiplet stacks and enable advanced system design and evaluation.
4. Integrated power and thermal management to reach efficiency and power density goals with modular designs for use with fine-pitch, bonded stacks of chiplets.

https://www.pcmag.com/news/nvidia-patent-suggests-3d-gpu-chip-stacking-tech-is-in-the-works
https://elements.envato.com/nichrome-filament-glowing-to-red-under-high-electr-JJGFDG7

Photonics and Connectors

- Connectors are high bandwidth, low latency, low energy per bit, low footprint components that allow multiple packaged subassemblies to communicate securely and error free.
- In a packaged system, connectors are expected to span a wide part of the electromagnetic spectrum depending on the distance to spanned.
  - Flexible active wired connectors for short distances
  - RF connectors for moderate distances
  - Photonic connectors for long distances
- We expect connectors to leverage the chiplet technology to the extent possible.
- It is expected that chiplet sub-assemblies-to-substrate connectors will be in scope.
- Traditional ball grid array (BGA) or land grid array (LGA) and conventional, wire bonds and silicon bridges are expected to be out of scope for funding.



Chiplets Ecosystem

- **Create better integrated highly reusable smaller chiplets at fine pitches***
  - Increasing performance by continually leveraging tighter bond pitch and closer interaction by fine-pitch packaging, starting at a bond pitch of ~10 microns.
  - Enables designs that consist of a discrete number of chiplets, include support for 3D stacks, and are based on a chiplet integration layer specification that is not adequately addressed in current open systems and reduces the cost of adding new chiplets.
  - System performance increased by scaling up the number of chiplets rather than by developing new larger chiplets.

Bond Pitch	Physical Integration	Logic Integration	Protocol Integration
50μ	✓	✗	✓
10μ	✓	✓	?
1μ	✓	✓	✗

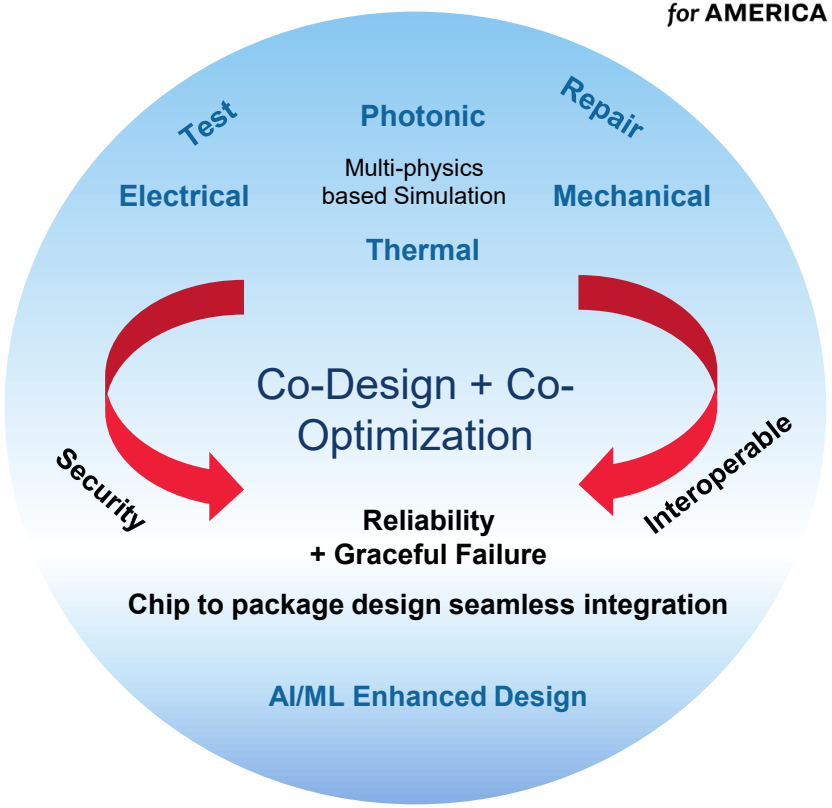
Integrate chiplets with EDA
(not protocols)

*CHIPS National Advanced Packaging Manufacturing Program (NAPMP) Briefing
https://www.nist.gov/news-events/events/chips-national-advanced-packaging-manufacturing-program-napmp-briefing

Co-design/EDA

Holistic package co-design “will be adapted for advanced packaging with consideration for built-in test and repair, security, interoperability, and reliability, with a detailed understanding of the substrate and processes used for assembly.”

- The intimate connection between chiplets and advanced packaging constructs requires a co-design platform that comprehends:
  - Chiplet architectures and communication options
  - Design for test, repair, security, and reliability especially “graceful failure”
  - Thermal and thermomechanical constraints
  - Substrate and assembly technology (no rework)



Co-design/EDA

Holistic package co-design “will be adapted for advanced packaging with consideration for built-in test and repair, security, interoperability, and reliability, with a detailed understanding of the substrate and processes used for assembly.”

The expected focus of this R&D area is co-design with automated tools of multi-chiplet subsystems for advanced packaging in scaled-down and scaled-out designs. Additional areas could include:

- The use of artificial intelligence/machine learning (AI/ML) in package design and design approaches for Test, Repair, Security, and Reliability including graceful failure.
- Innovations in EDA interoperability.
- Innovations in EDA automated flows for small chiplets, SoC, stack, and substrates, including synthesis, routing, timing, SI/PI/thermal analysis, verification, and security.
- EDA-enabled incorporation and co-optimization of chiplets of different sizes in a large platform design including logical electrical, photonic, thermal, and mechanical models; and advances in seamless integration of the chip to package.

National Advanced Packaging Piloting Facility (NAPPF)

NAPPF is planned to:

- be a U.S. facility where CHIPs funded development efforts will be transitioned and validated
- will have a set of tools that can support heterogeneous integration and “scale down and scale out”
- will be professionally staffed, with industry encouraged to propose research

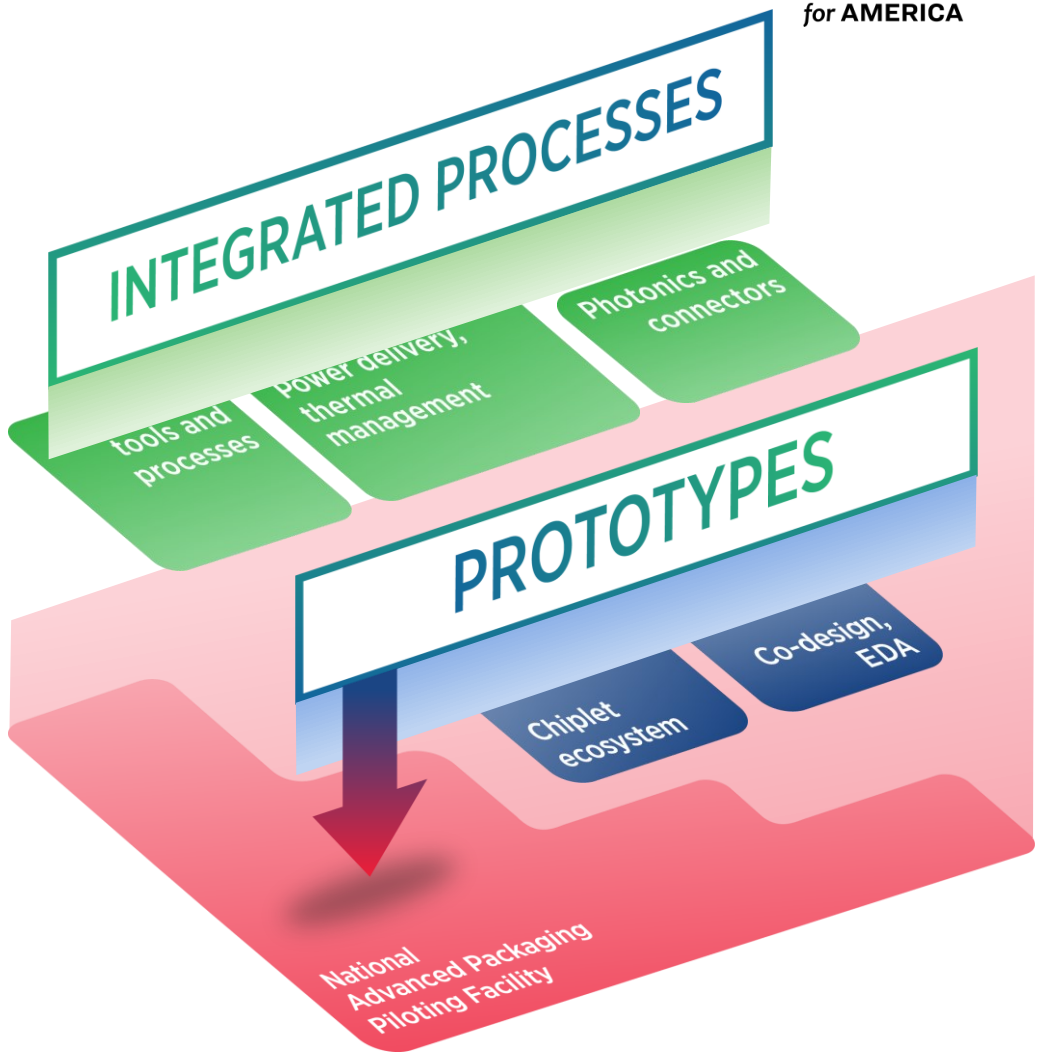
Technologies:

- NAPPF will start up with simplified end-to-end process flows based on 300mm Si or Glass
- Targeted applications are for High Performance and Low Power
- Prototypes developed in NOFO will be piloted in the NAPPF

Site Selection Process will be announced soon

An integrated approach

- The NAPPF* is a planned piloting and prototyping facility
- It will stand up as many as four exemplar processes. The NAPPF will include basic processes and source enhanced processes from the packaging community through NOFO2
- NOFO2 will include opportunities for high performance computing/AI and low power systems as exemplar packaging processes relevant to all R&D areas and prototyping.
- NOFO 2 includes provisions for prototypes - functional systems produced through an end-to-end advanced packaging process flow for the purpose of demonstrating the characteristics of that flow and the prototype design.



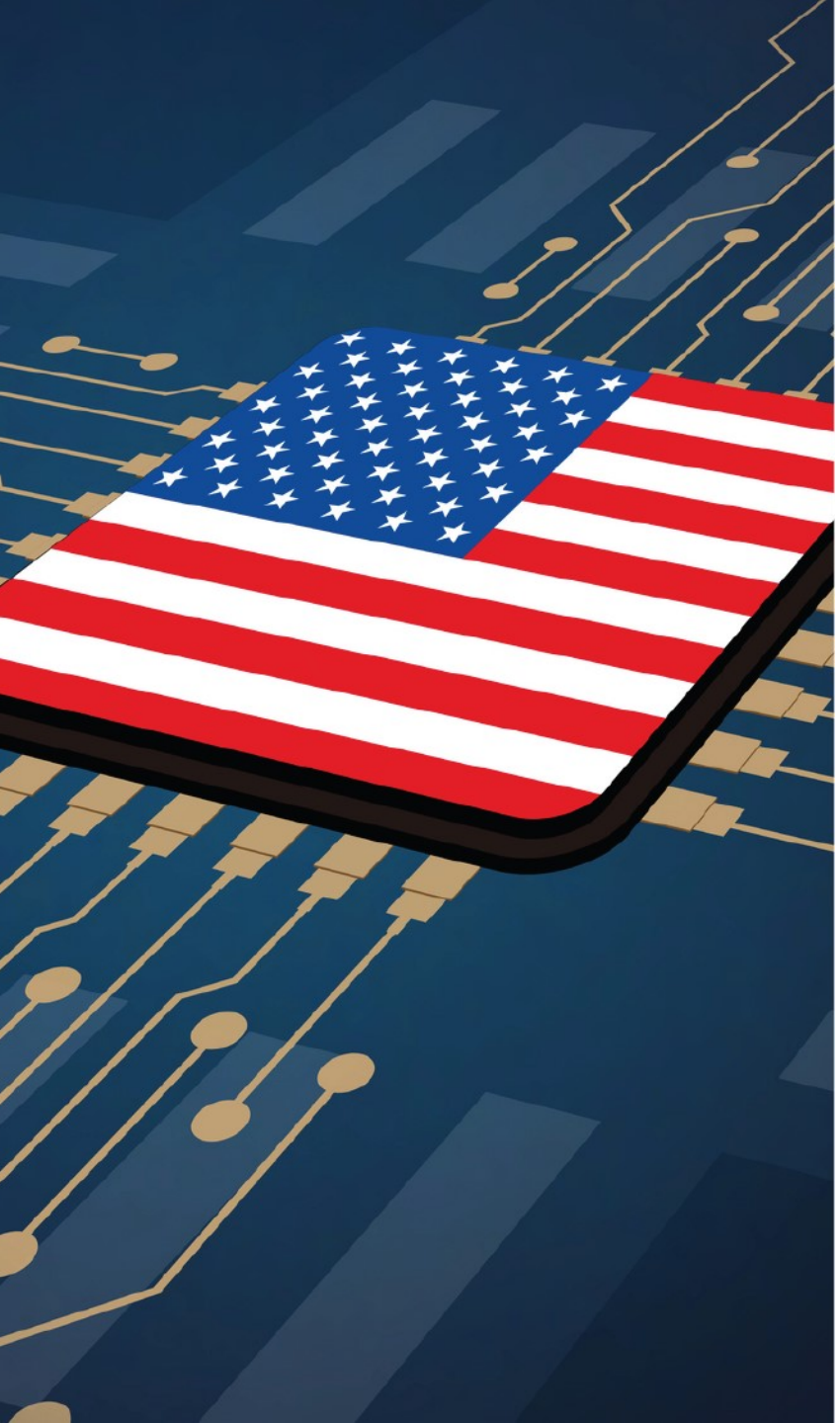
*NAPPF: National Advanced Packaging Piloting Facility

NOFO 2 Notice of Intent

FY2024 CHIPS R&D National Advanced Packaging Manufacturing Program (NAPMP) Advanced Packaging Research and Development

NOFO 2 NOI Summary

- Informed by
  - Industry Roadmaps (HIR, IRDS, MAESTRO, MAPT and MRHIEP)
  - Ongoing advances in High performance computing (including AI), Low Power Electronics (including medical applications)
- Funding Details
  - Total amount: Up to ~$ 1.6 Billion covering five R&D areas plus prototypes with advanced packaging flows to be implanted in the NAPPF
  - Individual awards up to ~$150 Million depending on scope
  - Co-investment encouraged
  - Eligible: Companies (profit & not-for-profit), educational institutions, state and local governments, FFRDCs – applicants must be domestic entities
  - NAPPF funding is excluded from this NOFO but technical areas must flow into NAPPF
- Teaming is essential in all areas



Next Steps

- Visit CHIPS.gov for resources, including:
  - Funding Updates List
  - Funding Opportunities
  - Vision for Success papers
  - Applicant Guides and Templates
  - FAQs and fact sheet
- Join our mailing list
- Contact us at askchips@chips.gov

Thank you!

askchips@chips.gov